

Claims

- [c1] 1. A silicon oxide gap-filling process, comprising:
providing a substrate having a trench thereon, wherein
an aspect ratio of the trench is 4.0 at least; and
performing a CVD process having an etching effect to fill
up the trench with silicon oxide, wherein reaction gases
used in the CVD process comprise deposition gases and
He/H₂ mixed gas as a sputtering-etching gas, wherein
the percentage of the He/H₂ mixed gas in the total reac-
tion gases is 70% at least.
- [c2] 2. The silicon oxide gap-filling process of claim 1,
wherein the CVD process comprises an HDP-CVD pro-
cess.
- [c3] 3. The silicon oxide gap-filling process of claim 1,
wherein a ratio of He to H₂ (He/H₂ ratio) in the He/H₂
mixed gas is 0.3–4.0.
- [c4] 4. The silicon oxide gap-filling process of claim 1,
wherein an ED ratio of the CVD process is 0.1–0.03.
- [c5] 5. The silicon oxide gap-filling process of claim 1,
wherein the deposition gases comprise SiH₄ and O₂.

- [c6] 6. The silicon oxide gap-filling process of claim 5, wherein in the CVD process, a flow rate of SiH_4 is 20–100sccm, a flow rate of O_2 is 40–200sccm, a flow rate of H_2 is 100–2000sccm, a flow rate of He is 200–2000sccm, a pressure is 5–20mTorr, a temperature is 400–650°C, a low-frequency RF power is 3000–15000W, and a high-frequency RF power is 500–5000W.
- [c7] 7. The silicon oxide gap-filling process of claim 1, which is applied to an STI process in a 90nm semiconductor process.
- [c8] 8. A silicon oxide gap-filling process, comprising:
providing a substrate having a trench thereon;
performing a CVD process having an etching effect to fill up the trench with silicon oxide, wherein reaction gases used in the CVD process comprise deposition gases and He/H_2 mixed gas as a sputtering-etching gas, and a percentage of the He/H_2 in the total reaction gases is raised with increase of an aspect ratio of the trench.
- [c9] 9. The silicon oxide gap-filling process of claim 8, wherein the CVD process comprises an HDP-CVD process.
- [c10] 10. The silicon oxide gap-filling process of claim 8,

which is applied to an STI process.

- [c11] 11. The silicon oxide gap-filling process of claim 8, wherein the aspect ratio of the trench is higher than 3, and the ratio of He to H_2 (He/ H_2 ratio) in the He/ H_2 mixed gas is 0.3–4.0.
- [c12] 12. The silicon oxide gap-filling process of claim 11, which is applied to an STI process in a semiconductor process under 0.13 μ m.
- [c13] 13. The silicon oxide gap-filling process of claim 11, wherein an ED ratio of the CVD process is 0.1–0.03.
- [c14] 14. The silicon oxide gap-filling process of claim 8, wherein the deposition gases comprise SiH_4 and O_2 .
- [c15] 15. The silicon oxide gap-filling process of claim 14 wherein in the CVD process, a flow rate of SiH_4 is 20–100sccm, a flow rate of O_2 is 40–200sccm, a flow rate of H_2 is 100–2000sccm, a flow rate of He is 200–2000sccm, a pressure is 5–20mTorr, a temperature is 400–650°C, a low-frequency RF power is 3000–15000W, and a high-frequency RF power is 500–5000W.
- [c16] 16. A silicon oxide gap-filling process, comprising:
providing a substrate having a trench thereon;

performing an HDP-CVD process to fill up the trench with silicon oxide, wherein reaction gases used in the HDP-CVD process comprise SiH_4 , O_2 , He and H_2 , wherein a flow rate of SiH_4 is 20–100sccm, a flow rate of O_2 is 40–200sccm, a flow rate of H_2 is 100–2000sccm, a flow rate of He is 200–2000sccm, a pressure is 5–20mTorr, a temperature is 400–650°C, a low-frequency RF power is 3000–15000W, and a high-frequency RF power is 500–5000W; an ED ratio of the HDP-CVD process is 0.1–0.03; and a percentage of the He/ H_2 in the total reaction gases is raised with increase of an aspect ratio of the trench.

- [c17] 17. The silicon oxide gap-filling process of claim 16, wherein the aspect ratio of the trench is higher than 3, and the ratio of He to H_2 (He/ H_2 ratio) in the He/ H_2 mixed gas is 0.3–4.0.
- [c18] 18. The silicon oxide gap-filling process of claim 17, which is applied to an STI process in a semiconductor process under 0.13 μm .
- [c19] 19. The silicon oxide gap-filling process of claim 17, wherein the aspect ratio of the trench is 4.0 at least, and the percentage of the He/ H_2 mixed gas is 70% at least.

[c20] 20. The silicon oxide gap-filling process of claim 19, which is applied to an STI process in a 90nm semiconductor process.